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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
| 10/511,566 | 04/13/2005 | Jurgen Leib | 2133.063USU | 4191 |
| 27623 | 7590 | 09/28/2009 | EXAMINER | |
| OHLANDT, GREELEY, RUGGIERO & PERLE, LLP | | | ARENA, ANDREW OWENS | |
| ONE LANDMARK SQUARE, 10TH FLOOR | | | ART UNIT | PAPER NUMBER |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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|------------------------------|--------------------------------------|------------------------------------|
| Office Action Summary | Application No. 10/511,566 | Applicant(s) LEIB ET AL. |
| | Examiner Andrew O. Arena | Art Unit 2811 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 14 May 2009.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1.3-10.12-17.19,20,34,39,41 and 43-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1.3-10.12-17.19,20,34,39,41 and 43-48 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

As a preliminary formal matter, the previous office action was indeed non-final.

The arguments filed 5/14/2009 were considered but are not persuasive.

The arguments allege several references are non-analogous, nevertheless, it is maintained that the combination relied upon for rejection is proper. Many glasses are generally known, and any art dealing with glass will be familiar with many glasses, including ones used in other field or disclosed in a reference alleged to be another field.

Claim Rejections - 35 USC § 103

Statute 35 U.S.C. § 103(a) is the basis for obviousness rejections made herein:

Claims 1, 3-7, 9, 10, 12-17, 45, 47 and 48 are rejected under 35 U.S.C. § 103(a) as unpatentable over Camlibel, Baglin and Sioshansi (all of record).

RE claims 1 & 45, Camlibel discloses a process for forming a housing for electronic modules, comprising the steps of:

providing a substrate (25 in Fig 2; 31 in Fig 3; 51 in Fig 4; 64/65/66 in Fig 5) having one or more regions, the one or more regions comprising at least one semiconductor structure (32/33; 52/53; 63), the substrate having at least a first substrate side (top) to be encapsulated and an underside, wherein the at least one semiconductor structure is located on the first substrate side;

providing a vapor-deposition ("E-beam deposition", col 4 ln 47-48) glass source ("glass target", col 4 ln 45-46);

arranging the first substrate side in such a manner with respect to the vapor-deposition glass source that the first substrate side can be vapor-coated (inherent); vapor-coating the first substrate side with a glass layer (col 4 ln 47-48); wherein the step of vapor-coating comprises the step of generating vapor by generating an electron beam and impinging the electron beam onto a glass target of the vapor-deposition glass source (col 4 ln 44-51).

Camlibel differs from the claimed invention in not explicitly disclosing the vapor-deposition arrangement and in not disclosing and ion beam for densification.

Baglin is analogous in applying insulating glass layers (title) to electronic modules (col 1 ln 41-45) such as those of Camlibel. Baglin discloses a plasma source (col 1 ln 58-60; col 4 ln 14-18) and the steps of producing an ion beam (17, col 4 ln 21) by ionizing a gas in a plasma generated by the plasma source (encompassed by a disclosure of "ions...include hydrogen, argon, xenon...", e.g., col 10 ln 18-20) and directing the ion beam onto the substrate to additionally densify the glass layer (col 2 ln 5-7; col 2 ln 12-15; col 4 ln 24-26), thus improving dielectric properties (col 11 ln 31-45).

Baglin does not explicitly disclose the glass source and plasma source in one arrangement and directing the ion beam onto the substrate during the vapor coating.

Sioshansi is analogous to Baglin in disclosing ion beam densification of deposited coatings (col 1 ln 7-11) and teaches directing the ion beam onto the substrate during the vapor coating (col 2 ln 5-7) wherein the glass source and plasma source can be provided in one arrangement (Fig 1). Sioshansi teaches that such a technique is "thought to offer many benefits" and "a most promising advance" (col 4 ln 6-29).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that, in view of Baglin and Sioshansi, the deposition of Camlibel utilize a glass source and plasma source in one arrangement, and comprise the steps of producing an ion beam by ionizing a gas in a plasma and directing the ion beam onto the substrate during the vapor coating; at least to densify the glass layer and improve dielectric properties using a known suitable arrangement.

RE claim 3, Camlibel discloses providing the substrate with a passivation layer (68) on a second side that is on the opposite side from the first substrate side.

RE claim 4, Camlibel discloses substrate comprises a wafer, the process further comprising packaging of components which still form part of the wafer (col 3 ln 45-47).

RE claim 5, Camlibel discloses vapor-coating a second substrate side with a glass layer (62 and 68 both glass; col 5 ln 63 – col 6 ln 2).

RE claim 6, Camlibel discloses the vapor-deposition glass source generates at least a binary glass system (col 3 ln 33-36, col 4 ln 8-10).

RE claims 7 & 9, Camlibel discloses the glass layer has any suitable and desired thickness (col 48-52), including an exemplary disclosure of 0.3 µm (col 7 ln 68).

RE claim 10, Camlibel discloses the glass layer has any suitable and desired thickness (col 48-52).

Camlibel differ from the claimed invention only in not expressly disclosing a glass layer thickness in the range between 50 and 200 µm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range between 50 and 200 μm ; at least to achieve a suitable desired thickness with predictable results.

RE claim 12, Camlibel does not particularly limit the borosilicate glass and therefore encompasses all well-known borosilicate glass types, including those containing aluminum oxide and alkali metal oxide fractions.

RE claim 13, Camlibel discloses the glass layer has a coefficient of thermal expansion that is virtually equal to that of the substrate (col 2 ln 57- 62; col 5 ln 7-18).

RE claim 14, Camlibel discloses the glass layer provides a hermetic seal.

RE claim 15, Camlibel discloses vapor depositing a plurality of glass layers onto the substrate (62, 68, col 5 ln 63 – col 6 ln 2).

RE claim 16, Camlibel discloses removing (e.g., polishing) material (of any type) from a second substrate side, the second substrate side being on the opposite side from the first substrate side (e.g., Fig 5 backside would be polished, as in col 6 ln 65).

RE claim 17, Camlibel discloses the substrate includes a wafer having a plurality of the structures wherein the process further comprises dividing the wafer to form a plurality of electronic modules which each have first encapsulated sides (col 3 ln 40-47).

RE claim 41, Camlibel discloses the semiconductor structure comprises an integrated circuit (col 3 ln 40-47).

RE claims 47 & 48, Camlibel as modified discloses a process, but does not explicitly disclose the temperature. A temperature must be chosen, and the skilled artisan is capable of selecting such temperature.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the temperature be maintained below 300 C and below 150 C during the vapor-coating of the glass layer; at least to use a suitable temperature.

Claims 8 and 46 are rejected under 35 U.S.C. § 103(a) as unpatentable over Camlibel, Baglin, and Sioshansi as respectively applied to claims 1 and 45, further in view of Butt (of record).

RE claim 8, Camlibel as modified above does not disclose organic constituents. Butt discloses that an organic-reinforced glass is particularly reliable and useful for hermetic sealing of electronic packages (col 2 ln 67 - col 3 ln 6, col 5 ln 11-17).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Camlibel in view of Butt by providing a reservoir having organic constituents and converting the organic constituents into the vapor state through the application of a vacuum so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side; at least for reliability.

Claims 19, 20, 34 and 39 are rejected under 35 U.S.C. § 103(a) as unpatentable over Camlibel, Baglin, and Sioshansi as for claim 1, further in view of Wada (of record).

RE claim 34, Camlibel differs from the claimed invention only in not explicitly disclosing the many processing steps embraced by his invention (col 3 ln 40-47).

Wada discloses (e.g., Fig 9) applying a layer of plastic (11) below the glass layer (9; ¶75 ln 5-7).

Camlibel in view of Wada differs from the claimed invention only in not disclosing said plastic layer on a surface of the glass layer opposite the substrate.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to reverse/rearrange the order of the glass layer and plastic layer; which would not modify the device operation. See MPEP § 2144.04(VI)(A&C).

RE claim 39, Camlibel differs from the claimed invention only in not explicitly disclosing the many processing steps embraced by his invention (col 3 ln 40-47).

Wada discloses (Figs 6) lithographing (¶85, ¶89) plastic layers (32, 42, 44) on the substrate and removing the plastic layers from the underside (Fig 6F-6G 44; ¶91 ln 1-2).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Camlibel in view of Wada to further comprise lithographing plastic layers on the substrate to define the structure and removing the plastic layers from the underside; at least to use known suitable processing steps to achieve a desired device having glass encapsulation.

RE claim 19, Camlibel in view of Wada discloses vapor coating the underside with the glass layer (Fig 11: 26) after the plastic layers (Fig 7F: 66) have been removed from the underside so that the plurality of electronic modules are encapsulated on both sides.

RE claim 20, Camlibel discloses the glass layer has any suitable and desired thickness (col 48-52).

Camlibel differ from the claimed invention only in not expressly disclosing a glass layer thickness in the range from 1 to 50 μm .

It would have been obvious to one of ordinary skill in the art at the time the invention was made that the glass layer have a thickness in the range from 1 to 50 μm ; at least to achieve a suitable desired thickness with predictable results.

Claims 43 and 44 are rejected under 35 U.S.C. § 103(a) as unpatentable over Camlibel, Baglin, and Sioshansi as for claim 1, in view of Harmon (US 3,204,023).

RE claims 43 & 44, Camlibel discloses the glass layer has a composition, in percent by weight, comprising a range of suitable SiO_2 and B_2O_3 fractions (Fig 1).

Camlibel differs from the claimed invention only in not explicitly disclosing the fractions of any trace compounds in the glass.

Many compositions of borosilicate glass are known in which contain the claimed compounds, e.g., Corning offers a plethora of compositions. Composition is known in the art to affect the coefficient of expansion and dielectric properties.

Harmon is evidence of the knowledge of ordinary skill in this art, and states that "well-known in the transistor art...a borosilicate glass comprised of...commonly known as Corning Glass 7052" (col 2 ln 70 – col 3 ln 10).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the glass layer has the claimed composition; at least to use an optimum glass composition.

Conclusion

The prior art made of record and not relied upon is considered pertinent.
Golecki and Champeau both disclose ion beam densification during vapor
coating in a single arrangement.

A sample of available Corning glasses and properties are listed from a catalog as
evidence of the many known properties and compositions in the art.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time
policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE
MONTHS from the mailing date of this action. In the event a first reply is filed within
TWO MONTHS of the mailing date of this final action and the advisory action is not
mailed until after the end of the THREE-MONTH shortened statutory period, then the
shortened statutory period will expire on the date the advisory action is mailed, and any
extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of
the advisory action. In no event, however, will the statutory period for reply expire later
than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the
examiner should be directed to Andrew O. Arena whose telephone number is (571)272-
5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on 571- 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew O. Arena/
Examiner, Art Unit 2811
14 September 2009

/Lynne A. Gurley/
Supervisory Patent Examiner, Art
Unit 2811